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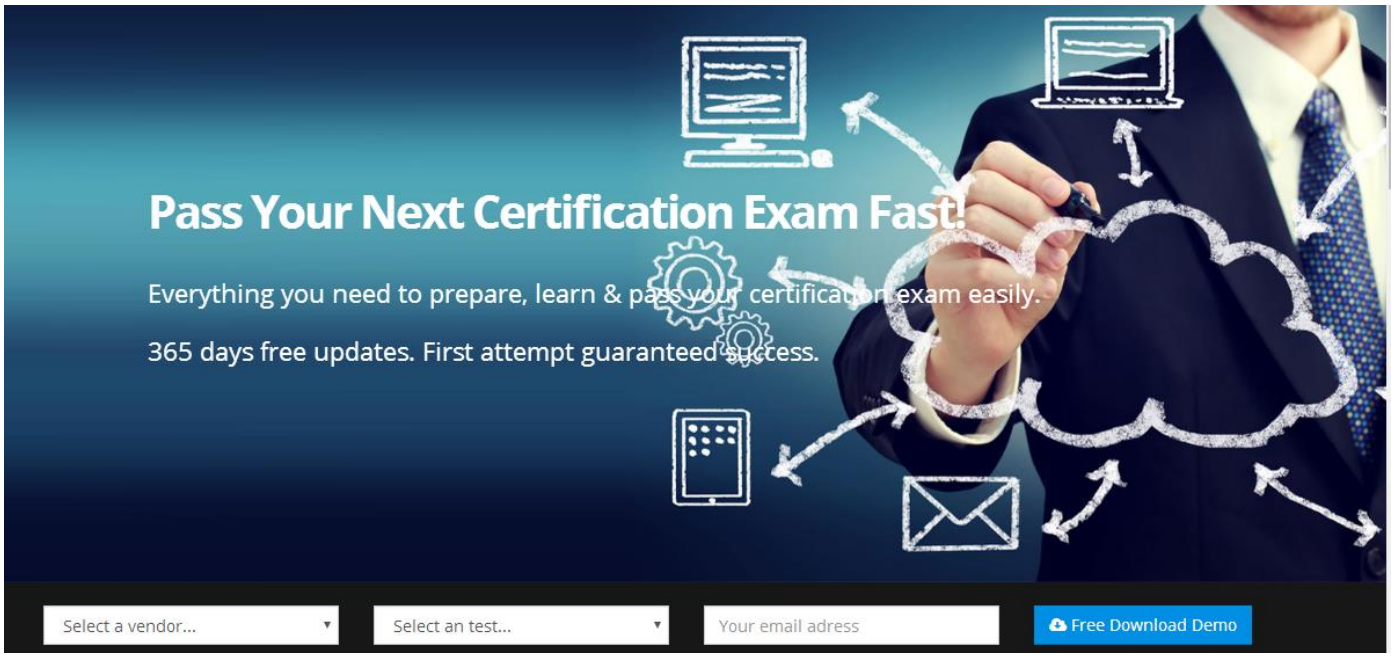

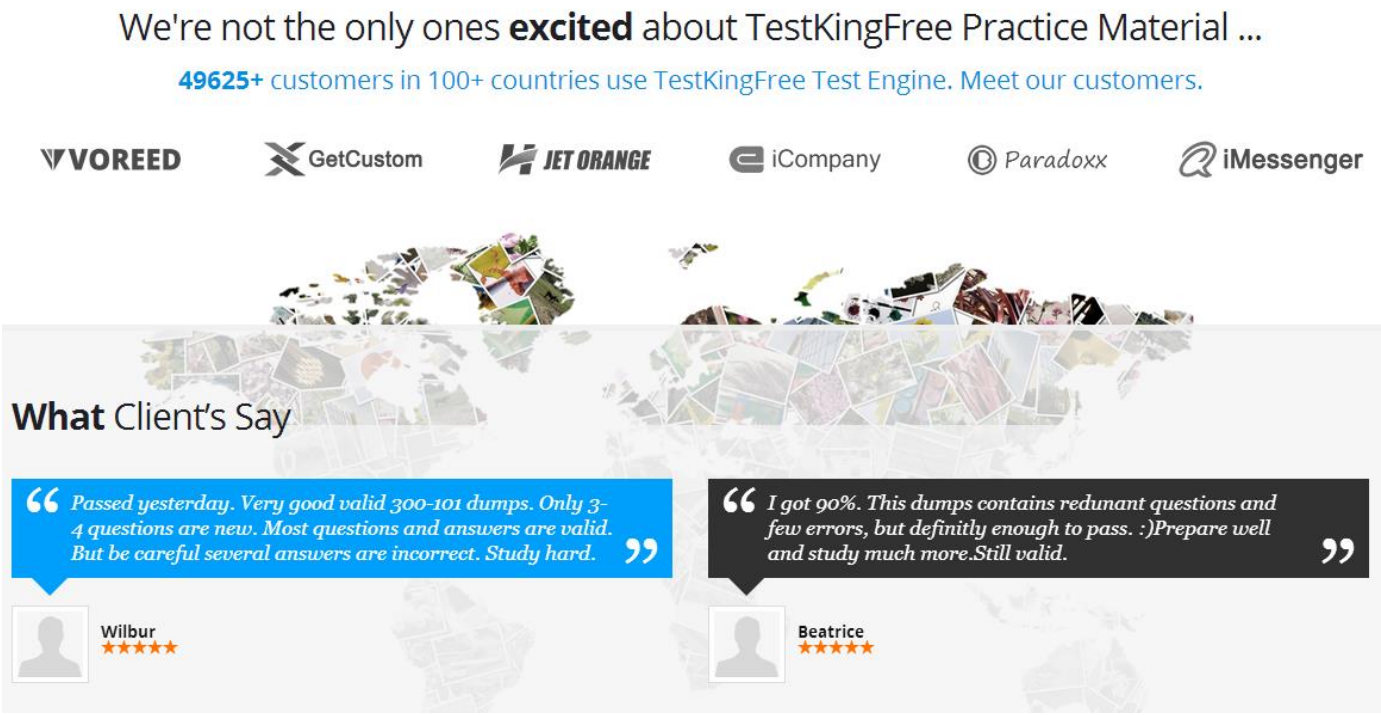

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Exam : **EN0-001**

Title : ARM Accredited engineer

Vendor : ARM

Version : DEMO

NO.1 In a Cortex-A9 processor, when the Memory Management Unit (MMU) is disabled, which of the following statements is TRUE? (VA is the virtual address and PA is the physical address)
A. VA == PA; No address translations; instructions and data are not cached
B. VA! = PA; No address translations; instructions may be cached but not data
C. VA == PA; Address translations take place; data may be cached but not instructions
D. VA == PA; No address translations; instructions may be cached but not data
Answer: D

NO.2 In the Generic Interrupt Controller (GIC), when an interrupt is requested, but is not yet being handled, it is in which of the following states?
A. Inactive
B. Active
C. Pending
D. Edge-triggered
Answer: C

NO.3 A simple system comprises of the following memory map:
Flash - 0x0 to 0x7FFF
RAM - 0x10000 to 0X17FFF
When conforming to the ABI, which of the following is a suitable initial value for the stack pointer?
A. Top address of RAM (0x18000)
B. Top address of flash (0x8000)
C. Bottom address of RAM (0x10000)
D. Bottom address of flash (0x0000)
Answer: A

NO.4 A program running on a development board that is connected to a host using a debugger can access a file on the host by using:
A. Memory mapping
B. Semihosting
C. Polling
D. Virtual I/O
Answer: B

NO.5 In which type of storage will the compiler preferentially place frequently accessed variables?
A. Stack
B. Heap
C. Registers
D. Hard disk
Answer: C

NO.6 What view in a debugger displays the order in which functions were called?
A. The Call Stack view
B. The Memory view

C. The Registers view
D. The Variables view
Answer: A

NO.7 Printf statements could be used to achieve which of the following debug tasks?
A. Observe changes to a local variable in a function
B. Capture a real-time trace of program execution
C. Debug boot code, before a call to the C main() function
D. Stop the processor at an interesting location in the code
Answer: A

NO.8 When the processor is executing in Thumb state, which of the following statements is correct about the values stored in R15?
A. Bits[31:16] are duplicated with bits[15:0]
B. The PC value is stored in bits[31:1] and bit[0] is treated as zero
C. The PC value is stored in bits[31:16] and bits[15:0] are undefined
D. The PC value is stored in bits[15:0] and bits[31:16] are undefined
Answer: B

NO.9 A standard performance benchmark is being run on a single core ARM v7-A processor. The performance results reported are significantly lower than expected. Which of the following options is a possible explanation?
A. L1 Caches and branch prediction are disabled
B. The Embedded Trace Macrocell (ETM) is disabled
C. The Memory Management Unit (MMU) is enabled
D. The Snoop Control Unit (SCU) is disabled
Answer: A

NO.10 When setting the initial location of the stack pointer and the base address of the heap, the ARM EABI requires that the:
A. Base address of the heap must be the same as the initial stack pointer.
B. Stack pointer must be 8-byte aligned.
C. Heap must be in external RAM.
D. Initial stack pointer must be the lowest addressable memory location.
Answer: B

NO.11 In an ARMv7-A processor, which control register is used to enable the Memory Management Unit (MMU)?
A. The ACTLR
B. The SCTLR
C. The TTBCR
D. The CONTEXTIDR
Answer: B

NO.12 A simple method of measuring the performance of an application is to record the execution time using the clock on the wall or a wristwatch.
When is this method INAPPROPRIATE?
A. When executing the software using a simulation model
B. When the processor is a Cortex-R4
C. When instruction tracing is enabled
D. When the processor is not executing instructions from cache
Answer: A